## REMARKS

This Application has been carefully reviewed in light of the Office Action mailed March 15, 2006. At the time of the Office Action, Claims 1-37 were pending in this Application. Claims 1-37 were rejected. Claims 1-37 have been canceled and new claims 38-74 have been added. Applicants respectfully request reconsideration and favorable action in this case.

### PTO Form 892

Applicants would like to bring to the Examiner's attention that certain claims have been rejected as being unpatentable over or anticipated by U.S. Patent 5,721,865 issued to Shintani et al. and U.S. Patent 5,483,552 issued to Shimazaki et al.; however, these references have not been identified on a PTO-Form 892, nor were they submitted by Applicants on a PTO-Form 1449. Applicants respectfully request that these references be listed on a PTO-Form 892 in the next action.

### Specification objections

Applicants have amended the specification to address the item object to by the Examiner. Applicants wish to thank the Examiner for identifying this item.

### Claim objections

Applicants believe that the claim objections are moot in view of Applicants' cancellation of claims 1-37.

### Rejections under 35 U.S.C. § 112

The Section 112, second paragraph rejections are moot in view of the cancellation of claims 1-37. Applicants believe that new claims 38-74 are compliant with Section 112, second paragraph.

**Rejections under 35 U.S.C. § 102(e)**

Claims 1-18 and 20-36 were rejected by the Examiner under 35 U.S.C. §102(b) as being anticipated by U.S. Patent 5,721,865 issued to Shintani. Applicants' cancellation of claims 1-37 moots the Section 102(e) rejection.

**Remarks regarding newly presented claims**

New independent claim 38 recites a device for controlling processing of data elements in which threads are assigned to data elements and no more than one data element enters the device at one time. The device includes a first unit for storing contexts associated with corresponding threads and for fetching a first unit instruction and entering the first unit instruction in a context associated with a thread assigned to an incoming data element. A second unit fetches a second unit instruction, which succeeds a stipulated instruction in a sequence of instructions of a stipulated thread. A third unit decodes either the first unit instruction or the second unit instruction and generates a control signal for processing of the data element.

Applicants respectfully submit that the cited reference does not teach or suggest the elements of claim 38 because the cited reference does not teach or suggest all of the claim limitations. For example, claim 38 recites a first unit for storing contexts associated with corresponding threads and for fetching a first unit instruction and entering the instruction in a context associated with a thread assigned to an incoming data element. The Office Action rejection of previously presented claim 1 states that Shintani discloses a first unit in which the context for each thread is entered and which fetches an instruction during a first clock cycle that is entered in the context of the thread assigned to the incoming data element. The portion of Shintani cited by the Office Action in support of this interpretation reads as follows:

> The prefetch unit 105 executes, based on prefetch control information initially set by the program executed by the processor 2, a group of data designated by the prefetch control information, e.g., look-ahead (prefetch) data of a plurality of elements in a certain array in asynchronism with an instruction execution performed by the processor 2.

Applicants respectfully submit that the cited portion of Shintani does not disclose or suggest the first unit as recited in Claim 38. Whereas claim 38 recites an instruction fetching

unit, the prefetch unit 105 of Shintani is a data prefetching device. See, e.g., Column 8, lines 36-38 "prefetch unit 105 prefetches a group of data designated by the prefetch control information under the control of a cache request unit 101." The fundamental and well known distinction between instruction prefetch and data prefetch is recognized by Shintani itself. For example, FIG. 11 of Shintani illustrates an instruction prefetch unit 1105A as a subcomponent of its general purpose processor 2. In contrast, the data prefetch unit 105 of Shintani is a physically distinct unit that is external to processor 2. Whereas an analogy between instruction fetching first unit of new claim 38 and Shintani's instruction fetching unit 1101A might be defensible, the Office Action's attempt to equate the claimed instruction fetching unit with the reference's data prefetching unit is not.

In addition, claim 38 recites that its first unit is operable for storing contexts associated with corresponding threads. The Office Action's rejection of previously presented claim 1 indicates that Shintani discloses a first unit in which the context for each thread is entered. The Office Action supports its assertion relying on the same passage quoted above and states that the "instruction is fetched according to control information that is set, whereas a thread is viewed as a collection of threads."

To the extent that the Office Action is drawing an analogy between Shintani's prefetch control information and the context information recited in previously presented claim 1 and newly presented claim 38, Applicants respectfully disagree with the analogy. The Shintani prefetch control information is information that is stored in Shintani's processor that controls the manner in which data is prefetched. The Shintani prefetch information, for example, designates the length of an operand used in a memory access instruction. In other words, the Shintani prefetch information are processor parameters that the processor uses to control the manner in which data is prefetched. In contrast, the context information recited in claim 38 is entered in the first unit itself and describes a state of the corresponding thread. Thus, the cited reference does not disclose or suggest a first unit in which context information is stored as recited in claim 38.

Moreover, new claim 38 recites that a third unit selects the instruction to be decoded from either the first unit instruction or the second unit instruction. The Office Action rejection of previously presented claim 1 indicates that Shintani discloses a third unit (a

decoder) and a pipeline "which embodies the three units connected." Assuming for the sake of this discussion that Shintani does disclose a connecting pipeline, Shintani does not disclose where the third unit selects its instruction for decoding from either the first unit or the second unit. The functional connection between the first, second, and third units as recited in claim 38 is simply not taught either expressly or inherently by the cited reference.

Because the cited reference does not disclose either expressly or inherently all elements, of claim 38, Applicants respectfully request the Examiner to consider and take favorable action on claim 37 and all of its dependent claims.

With respect to new independent claim 57, Applicants submit that the claim is allowable over the cited reference for reasons paralleling the reasons advanced above with respect to claim 38.

**Rejections under 35 U.S.C. §103(a)**

Claims 19 and 37 were rejected under 35 U.S.C. §103(a) as being unpatentable over Shintani in view of U.S. Patent 5,483,552 issued to Shimazaki et al. ("Shimazaki"). Both claims have been canceled. New claim 56, however, recites elements analogous to previously presented claim 19. Applicants submit that claim 56 is patentable over the cited references because the cited references do not teach or suggest all of the claim limitations. Shimizaki is cited merely for its reference to delay elements. Shintani, as discussed above, does not disclose or suggest the elements of claims 56 inherited from base claim 39. Accordingly, the cited references do not teach or suggest all of the claim limitations.

**Newly presented claims**

Applicants have presented new independent claim 73 and new dependent claim 74. Applicants request examiner and favorable action with respect to these claims.

**Association of Customer Number and Change of Correspondence Address**

Applicants respectfully request that all papers pertaining to the above-captioned patent application be associated with Customer No. **58174**, and direct all correspondence pertaining to this patent application to practitioners at Customer Number **58174**. All telephone calls should be directed to Joseph P. Lally at 512.322.2680.

## CONCLUSION

Applicants believe this case is in condition for allowance in light of the amendments and remarks set forth above. Applicants respectfully request favorable action on all pending claims.

Applicants enclose a Petition for One Month Extension of Time and authorize the Commissioner to charge the $120.00 extension fee to Deposit Account No. 50-2148 of Baker Botts L.L.P. Applicants believe no further fees are due, however, the Commissioner is hereby authorized to charge any other fees necessary or credit any overpayment to Deposit Account No. 50-2148 of Baker Botts L.L.P.

If there are any matters concerning this Application that may be cleared up in a telephone conversation, please contact Applicants' attorney at 512.322.2680.

Respectfully submitted,
BAKER BOTTS L.L.P.
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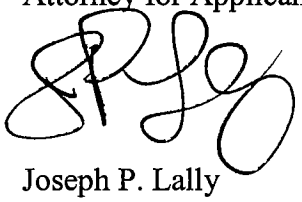

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Date: July 13, 2006

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